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COMPENSATION OF 2nd HARMONIC DISTORTION IN A 4-FET LINEARISED TRANSCONDUCTOR CIRCUIT

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ABSTRACT

In this paper, a method of compensation for the 2nd harmonic distortion of a 4-FET linearised transconductor circuit is proposed and evaluated. The sensitivity of the 2nd harmonic distortion level to the compensation parameters is evaluated. Taking account of integrated circuit process parameters, it is concluded that compensation is possible for wide bandwidths up to a decade in frequency. As a first step in understanding the mechanism causing distortion in the circuit, an expression and set of curves showing the effect of signal mismatch in a FET-pair is presented, but we identify the fact that further work is needed.

1 INTRODUCTION

In [1] a general synthesis method has been presented for transconductor/multiplier circuits using Gallium Arsenide (GaAs) MESFETs. The circuits synthesised include generalised transconductors (inverting, non-inverting, differential input, tunable) and 4-quadrant multipliers (single term, double term, quadruple term, differential input, double differential input). The synthesis is based on a very simple model for the GaAs MESFET

$$I_d = \beta (V_{gs} - V_T)^2 \quad (1)$$

It has been recognised that circuits derived from the synthesis will require some form of compensation for aspects of real FET behaviour beyond that described by (1). At low frequencies, the most dominant effect not included in (1) is finite FET drain-source conductance and two approaches to this problem have been considered.

In [2], cascode transistors are introduced into a 4-quadrant multiplier circuit derived in [1], but this increases power supply voltage and involves a considerable increase in circuit complexity. In [3], a different approach is adopted to compensate the 2nd harmonic distortion of a 4-FET linearised transconductor [4,1]. This approach employs a cancellation of the squared term in (1) that depends on close matching of complementary voltages supplied to gate-source ports of a sink-FET and a source-FET [1]. The effect of finite FET drain-source conductance will be to cause mismatch of these voltages, but it is accordingly proposed in [3] that signal balance can be restored by making alterations to the gate-widths of the FETs [1]. For the 4-FET linearised transconductor, this technique was shown to be effective for a 100 MHz signal using a new GaAs MESFET model [5,6] implemented in the SPICE3e circuit simulator. It has since been observed that this method of compensation becomes less effective at higher frequencies. This effect is attributed to the parasitic capacitances associated with the FETs.

The purpose of this paper is to report further progress in the compensation of transconductor/multiplier circuits using FETs. We use the 4-FET linearised transconductor of [4] as an illustrative example. We begin by presenting a generalised analysis of the effect of errors in the amplitude and phase of the gate source voltages of the source and sink MESFETs. The results lead to a proposal for an improved compensation technique. This is evaluated using SPICE and the sensitivity of the compensation is examined. Finally, we

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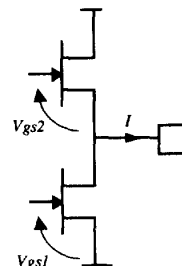


Fig 1: Source-FET sink-FET pair

consider analytical prediction of the distortion of the transconductor circuit.

2 ANALYSIS OF SIGNAL MISMATCH FOR FET-PAIR

The source-FET sink-FET pair of Fig 1 forms the basis of the linearised transconductor circuits in [1]. The gate-source voltages of the FETs can be described by

$$\begin{aligned} V_{gs1} &= V \sin \omega t \\ V_{gs2} &= -\alpha V \sin (\omega t + \phi) \end{aligned} \quad (2)$$

where α is an amplitude error factor and ϕ is the phase error. Assuming the simple FET model of (1), the output current I contains a dc term, a linear term and a 2nd order term. The magnitude of the 2nd order term normalised to the magnitude of the linear term for $\alpha = 1$ and $\phi = 0$ is given by

$$|D_{20}| = \frac{1}{8} \frac{V}{V_T} \sqrt{\alpha^4 + 1 - 2\alpha^2 \cos 2\phi} \quad (3)$$

Equation (3) shows that the 2nd harmonic component of I is zero only for gate-source voltages that have identical amplitude ($\alpha = 1$) and opposite phases ($\phi = 0$). Equation (3) can be used to evaluate the effect of gain and phase errors on distortion. Equation (3) can also be used to estimate the tolerance on gain and phase matching required to achieve a given minimum distortion level specification, all assuming the simple FET model in (1).

The effect of gain and phase errors determined with a more detailed FET model is illustrated in Fig 2, which shows the 2nd harmonic distortion in I relative to the fundamental for the FET-pair of Fig 1. The FET model used is that of [5,6] with parameters values chosen to model a typical TriQuint GaAs depletion-mode MESFET, which has a threshold voltage of -0.7 V and an f_T of 11 GHz. This model has been shown to accurately predict the measured distortion of this FET [6]. It has been shown that the curves in Fig 2 follow the data derived from (3) based on the simple model of (1) to within ± 2 dB.

Fig 2 illustrates that 2nd harmonic distortion is critically dependent on the phase error of the source and sink MESFET gate-source voltages as well as on the amplitude error. This leads us to consider a transconductor circuit compensation technique in which both phase and amplitude of the gate-source voltages are defined as precisely as possible over maximum bandwidth.

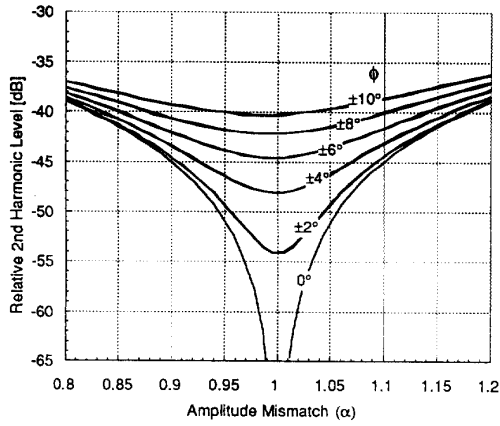


Fig 2: Effect of amplitude mismatch factor α and phase error ϕ

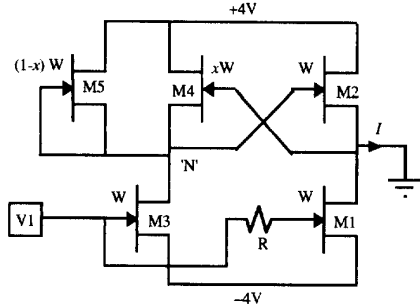


Fig 3: 4-FET linearised transconductor with R-x compensation

3 TRANSCONDUCTOR COMPENSATION

The compensated 4-FET transconductor of [4] is shown in Fig 3. The compensation parameters are the resistance R and the parameter x , which determines the gate-widths of MESFETs M4 and M5. With $R = 0$, the circuit becomes identical with the partially compensated circuit of [3] and with $R = 0$ and $x = 1$, it reverts to the uncompensated circuit of [4]. FET M5 of width $(1-x)W$ is not present in the original transconductor of [4] but is include in [3] and here in order to ensure that the dc input offset voltage of the circuit remains zero for any value of the compensation parameter x .¹ The circuit is shown in its dc-coupled form with gate-source bias voltages of 0 V. The compensation technique is equally applicable to the ac-coupled version of the circuit [7]. At this stage, for simplicity, the transconductor is assumed to be terminated at its output in a short-circuit and to be excited by a voltage source.

The argument behind the proposed method of compensation is as follows. First consider the circuit in an uncompensated state ($x = 1$ and $R = 0$) and with FETs described by (1). In this situation V_{gs4} (gate-source voltage of M4) is equal to V_{gs3} and, by virtue of the cross-coupled connections, $V_{gs2} = -V_{gs4} = -V_{gs3}$. Since $V_{gs1} = V_{gs3}$, the source and sink FETs (M2 and M1) have complementary gate-source voltages, which is the condition required for linearisation [1] and is illustrated in Fig 2.

At low frequencies, finite drain-source conductance of the FETs should be considered. The effect of this will be to reduce the

¹In practice, M5 may be omitted with a slight adjustment made to the other FET gate-widths to restore zero dc offset.

Table 1: Simulated distortion levels for compensated and uncompensated transconductor

Frequency [GHz]	Harmonic	Uncompensated Level [dBm]	Compensated	
			Level [dBm]	R and x
0.1	1	0.0	0.15	$R = 40\Omega$ $x = 0.525$
	2	-34.6	-65.0	
	3	-62.3	-55.9	
	4	-97.2	-82.8	
0.2	1	0.0	0.15	$R = 45\Omega$ $x = 0.538$
	2	-34.7	-64.9	
	3	-59.8	-55.0	
	4	-91.7	-82.9	
0.5	1	-0.1	0.00	$R = 45\Omega$ $x = 0.550$
	2	-35.2	-72.8	
	3	-55.0	-52.1	
	4	-84.0	-81.8	
0.7	1	-0.2	-0.16	$R = 45\Omega$ $x = 0.563$
	2	-35.7	-67.7	
	3	-53.4	-51.2	
	4	-81.9	-80.9	
1.0	1	-0.5	-0.55	$R = 55\Omega$ $x = 0.613$
	2	-36.6	-70.6	
	3	-52.3	-51.3	
	4	-80.9	-79.1	
1.5	1	-1.0	-1.51	$R = 65\Omega$ $x = 0.775$
	2	-37.6	-69.2	
	3	-52.4	-53.7	
	4	-82.9	-79.2	

magnitude of V_{gs4} and hence of V_{gs2} . The parameter x has been used in [3] to increase V_{gs4} until the gate-source voltage of the source FET has the correct magnitude.

At high frequencies, we should consider the FET parasitic capacitances, of which the gate-source capacitance is dominant. Assuming initially that these capacitances are linear (constant), then C_{gs4} (C_{gs} of M4) and C_{gs2} are connected in parallel at node 'N' and will produce a pole at $g_m/(2C_{gs}) (= f_T/2)$ in V_{gs4} and hence in the gate source voltage V_{gs2} of the source FET. This pole will increase the phase of the gate source voltage of the source FET at high frequencies. The introduction of the now proposed compensation resistor R in Fig 3 introduces a matching pole in the expression for the gate-source voltage of the sink-FET V_{gs1} by virtue of its gate-source capacitance C_{gs1} . Thus R (together with x) may be chosen such that the gate-source voltages of the source and sink FETs are matched in amplitude and phase over an extended frequency band. On the basis of this simple theory, the required value for R is $2/g_m$.

4. EVALUATION OF COMPENSATION TECHNIQUE

The above compensation method was evaluated by simulating the harmonic distortion of the circuit in Fig 3 using SPICE3f2 [8]. The FET model was that for TriQuint DFETs as described in Section 2. The transconductor was terminated at its output in a 50 Ω resistor and its input port was driven by a 50 Ω resistive source. The FET gate width parameter W in Fig 3 was 200 μm giving a gain for the circuit of 3.55 dB. The signal level was set to give an output signal level of 0 dBm. For the gate-width chosen, the value of the compensation resistor R , according to the simple theory in Section 3, is 85 Ω .

The level of the harmonic distortion components in the output current I of the uncompensated circuit ($x = 1$ and $R = 0$) is given in Table 1 for chosen frequencies. It can be seen that the highest level component apart from the fundamental is the 2nd harmonic.

Figs 4a, b and c show 3-dimensional graphs of 2nd harmonic distortion level versus R and x for frequencies of 0.2, 1 and 1.5 GHz. The graphs show 2nd harmonic distortion level relative

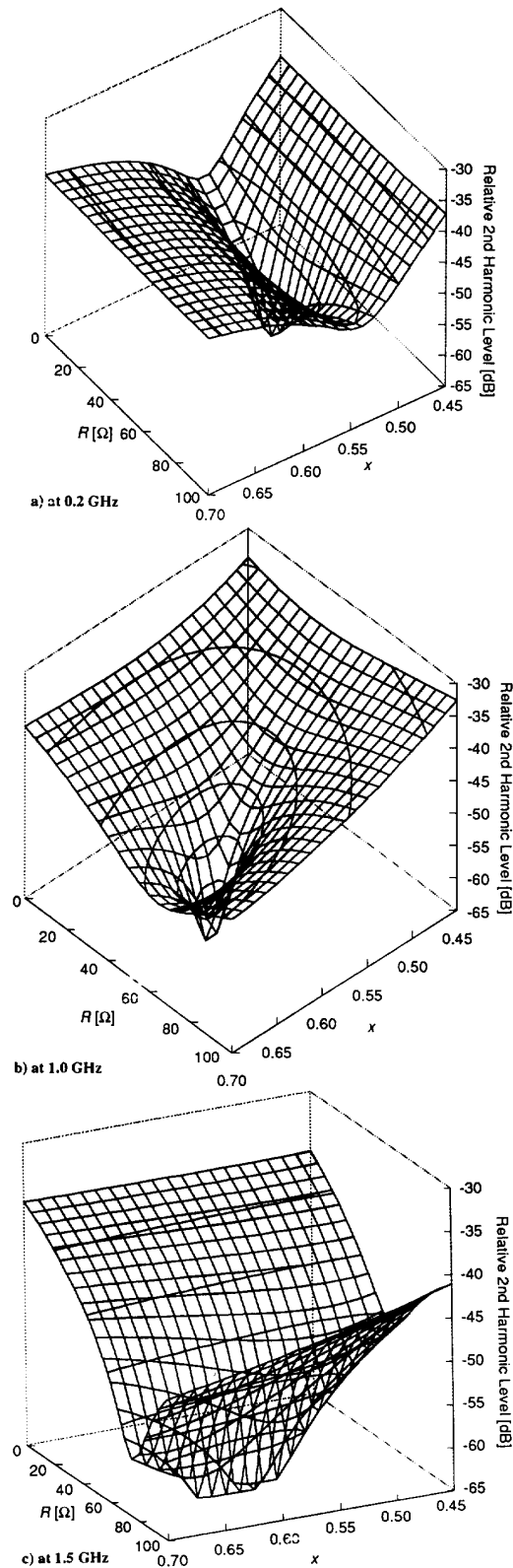


Fig 4: Computed relative 2nd harmonic level for transconductor as a function of both compensation parameters

Table 2: Observations and conclusions for contour plots

	Observation	Conclusion
A	As distortion level decreases, the contours become smaller and there is less tendency for overlap	A more stringent distortion level requirement reduces the possible bandwidth
B	As frequency increases the vertical axis of the pseudo-elliptical contours decreases and the horizontal axis increases	An increase in sensitivity to R and reduction in sensitivity to x with frequency is implied
C	The smallest contours (for the -60 dB level, Fig 5c) correspond to tolerance boxes yielding required tolerances for R and x of approximately 14 % and 3 %, respectively	Bearing in mind typical process tolerances on FET gate width matching and resistor value, it is implied that 2nd harmonic levels less than -60 dB at the spot frequencies given are feasible
D	Fitting a tolerance box into the shaded intercept region in Fig 5a yields tolerances of 10 % and 2 % in R and x , respectively	For a 2nd harmonic level below -50 dB and likely process tolerances, a bandwidth of 100 MHz to 1 GHz is feasible
E	Fitting a tolerance box into the shaded intercept region in Fig 5b yields tolerances of 15 % and 1.2 % in R and x , respectively	For a 2nd harmonic level below -55 dB and likely process tolerances, a bandwidth of 100 MHz to 700 MHz is feasible
F	Fitting a tolerance box into the shaded intercept region in Fig 5c yields tolerances of 20 % and 0.7 % in R and x , respectively	For a 2nd harmonic level below -60 dB and likely process tolerances, a bandwidth of 100 MHz to 500 MHz is feasible although the tolerance on x will be critical

to the fundamental level. At these frequencies, the 2nd harmonic can be effectively compensated by appropriate choice of compensation parameters. The optimum compensation parameter values are given in Table 1. The value of R is frequency dependent and significantly less than the predicted value of 85Ω ; this will be discussed later.

The harmonic distortion levels at the chosen frequencies for the compensated circuit are also given in Table 1. It can be seen that compensation of the 2nd harmonic does cause some increase in 3rd harmonic but this becomes insignificant at higher frequencies; ongoing work is aimed at simultaneous compensation of 2nd and 3rd harmonic components and therefore the increase in 3rd harmonic is not regarded as a long-term problem.

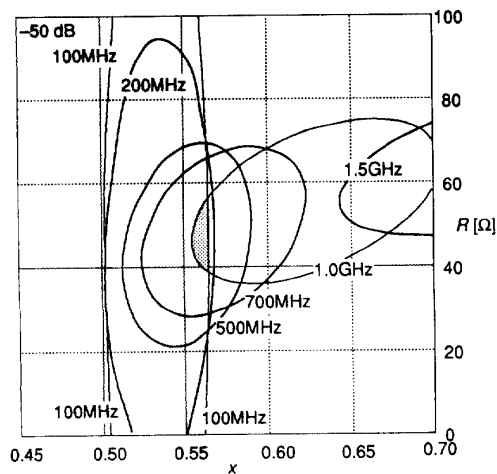
5 SENSITIVITY OF DISTORTION TO COMPENSATION PARAMETERS

For any compensation technique, it is important to determine the required tolerance on the compensation parameters and to compare them with the likely process tolerances to be encountered in fabrication. The sensitivity of the 2nd harmonic distortion of the transconductor to the compensation parameters R and x is shown by contours corresponding to the intersection of the 3-dimensional surfaces in Fig 4 with horizontal planes representing given distortion levels. All R - x points enclosed by a given contour provide a 2nd harmonic below that of its corresponding level.

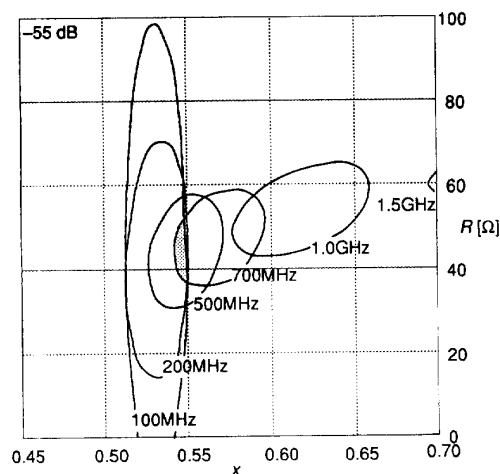
The contour plots obtained are shown in Figs 5a, b and c for distortion levels of -50 dB, -55 dB and -60 dB, respectively. From these graphs, we make the observations shown in Table 2 together with resulting conclusions. The conclusions in Table 2 are regarded as encouraging since they confirm the basic feasibility of compensating the 2nd harmonic distortion of the circuit.

6 PREDICTION OF CIRCUIT DISTORTION

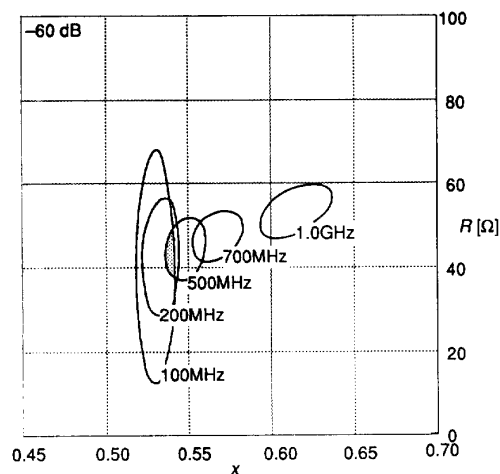
Having empirically proven the compensation technique by means of SPICE simulation, it is important to try to predict the values of the compensation parameters analytically in order to confirm our understanding of the distortion mechanism and its compensation. We have already seen that the optimum value of the compensation resistor R differs from the value predicted by the very simple theory presented in Section 3. The next step is to investigate the theory on effect of signal mismatch on distortion developed in Section 2.



a) for -50 dB



b) for -55 dB



c) for -60 dB

Fig 5: Contours of compensated transconductor's 2nd harmonic distortion level

Table 3: Simulated and predicted distortion

Frequency [GHz]	α	ϕ [°]	2nd Harmonic Level [dB]	
			Eq. (3)	SPICE
0.1	0.61	1.4	-35.0	-34.6
0.2	0.61	2.9	-35.0	-34.7
0.5	0.61	7.2	-34.8	-35.1
0.7	0.61	10.1	-34.5	-35.5
1.0	0.60	14.3	-34.0	-36.1
1.5	0.59	21.2	-33.1	-36.6
2.0	0.57	27.8	-32.3	-36.3

Table 3 shows amplitude and phase mismatch factors determined by SPICE for the gate-source voltages of the source and sink MESFETs in the transconductor circuit at a range of frequencies. Table 3 also shows the resulting 2nd harmonic distortion due to signal mismatch predicted by (3) as well as the simulated 2nd harmonic distortion figures copied from Table 1. It can be seen that there is a discrepancy between the two sets of figures and that whereas the simulated 2nd harmonic decreases with frequency, that predicted increases.

Thus the signal mismatch theory does not provide a complete explanation of the distortion in the uncompensated circuit and therefore cannot be used to predict the values of the compensation parameters. We are forced to conclude that another mechanism must be primarily responsible for the observed distortion. The identification of this mechanism and the prediction of the compensation parameter values are to be the subject of further work.

7 CONCLUSIONS

The method for compensation of 2nd harmonic distortion presented has exploited beneficial degrees of freedom which the 4-FET linearised transconductor circuit inherently provides. The method has been proven using models of TriQuint foundry MESFETs implemented in SPICE. The tolerances required for the compensation parameters are compatible with expected process variations. Further work is needed to understand the distortion mechanism operating in the circuit in order to correctly predict the values of the compensation parameters. In practice, 3rd harmonic distortion can be more serious than 2nd harmonic distortion because it produces in-band frequency components. An important task of ongoing work will be to study distortion methods for 3rd harmonic distortion.

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