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AUTOMATIC DESIGN OF GaAs DIGITAL CIRCUITS AND DEVICES - FROM PROCESS AND MATERIAL PARAMETERS TO LAYOUT

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ABSTRACT

Sydney University Electrical Engineering and CSIRO Division of Radiophysics have collaborated over the past three years to develop the design techniques and tools needed to build optimised digital circuits for MBE processes geared to low noise microwave and millimetre wave applications. The design approach commences with input of the fundamental process parameters and design rules. From these, SPICE models suitable for use in the design of both linear and digital circuits are automatically generated. These, in turn, are used to automatically design and layout basic logic gates. Simplified models of the gates are extracted for use with a mixed-mode simulator. This entire task from designer entry of parameters, through generation of accurate and simplified models, to layout, can be completed in less than 90 minutes. This paper gives an overview of the design process, describes each of the key problems that had to be addressed in its automation, and shows results of a fabricated circuit.

INTRODUCTION

The major part of the start-up effort in designing GaAs digital integrated circuits for a new technology is in the creation of re-useable resources including model and layout libraries of devices, logic gates and common standard cells. Even relatively minor technology changes may necessitate alteration or complete re-creation of these resources. During our development of digital circuits, the continuing evolution of the fabrication process has dictated a resource development approach that readily accommodated change. The design system described here is our tool for automatically creating circuit design resources.

DESIGN TOOLS AND STANDARD LIBRARIES

Fundamental to the digital circuit design process is the set of CAD tools used to assemble and simulate circuits. Simulation tools use appropriate device and circuit models, and layout tools use fabrication design rules. Small custom cells and circuits are designed using discrete device models with the aid of an accurate physical level circuit simulator. Larger circuits require a system level simulator using simplified models.

The CAD tools draw on a library containing appropriate models for simulating a circuit and a set of subcells for laying out the chip mask. The library includes a standard set of logic func-

tions with a range of power and speed characteristics. Each library element is represented in three forms: a physical simulator model based on discrete devices, a system model for rapid large-circuit simulation, and a mask layout description. Also required is a set of discrete device models for the design of custom elements and for use with the library physical models.

The basic tools used in our system are:

SPICE. The SPICE [1] circuit simulator uses device or physical level modeling. Library cell models and a set of device models including parasitic elements are used for designing custom circuits and for the development of system level models.

Simulation JIG. The Simulation JIG [2] is a mixed-mode (analogue/gate/behavioural) simulator. It uses simple models that represent the active circuit elements between an input node and an output node by a current source, a conductance, a capacitance at the output node and a capacitance at the input node. These components have values which are simple piecewise linear functions of potentials at the output and input nodes. This provides a rapid system-level simulation and uses the simple system-level models for each basic gate element in the cell library.

Magic. The mask layout tool, *Magic* [3], includes design rule checking and circuit extraction functions. It can be used to layout custom circuits (including library cells) and assemble subcells from the circuit library. The design rules for the fabrication process are used by the checking and extraction routines.

DESIGN APPROACH

The design system follows a logical design flow from fundamental parameters through to an automatic design of logic gates. Design commences with the input of fundamental material and process parameters, and design rules. This starting point gives flexibility for adapting to a fundamental change of technology and provides a means to consider the affect of process variations on the final circuit elements. Sensible default parameters are available at all stages so that the designer may take up the design sequence at any stage. Moreover, derived (calculated) values may be over-ridden by those obtained from measurement. If the process is known, the appropriate parameters can be entered and device models will be generated. If measured device parameters are available, the process parameters can be by-passed and the design sequence can start with entry of the device descriptions.

Implementation of the design system required the development of the rules and procedures for creating device descriptions

and circuit elements from fundamental parameters. Hence, the parameters which define the fabrication process had to be identified. Also, it was necessary to supplement the design tools noted above with specific models and routines for handling the new devices and GaAs technology.

Process Dependent Parameters

Starting with the fabrication process parameters provides three advantages. Firstly, because the design sequence is automated, a change in the fabrication process can be painlessly re-applied to update an entire circuit library. Secondly, the design sequence starts at a fundamental level so it can be quickly adapted to a fundamental change such as a change of material, from GaAs to InP for example, or moving from a MESFET to a HEMT technology. Thirdly, the design system becomes a valuable tool for determining the effect of process variations on the final circuit elements.

The fundamental parameters listed in Table I can be divided into three categories: material dependent, process dependent and design dependent.

Material Parameters. The crystal and electron transport properties of the material, be it silicon or a III-V compound are required to determine the electrical behaviour of the devices manufactured with it. These properties are not affected by subsequent fabrication steps. However, they are affected by design parameters such as the choice of nominal doping level, so the design system must be able to predict these influences.

Process Parameters. Process changes affect the quality of Schottky junctions and ohmic contacts. The Schottky metal chosen is significant and its properties are required to predict Schottky barrier heights and ideality. Alloyed ohmic connections vary with the contact geometry so several parameters measured from process samples are required to predict contact resistance [4]. Also, the minimum electrode spacing is restricted by the alignment and lithography tolerances. These parameters are dictated by the capabilities of the fabrication process and they are independent of the type of device constructed with the process. Mask layout design rules are also dictated by the process.

Design Parameters. Devices used for a particular circuit can be tailored to the application by setting the design parameters. MESFET pinch-off potential, for example, is adjusted by setting the channel depth. Parasitic resistances and capacitances are affected by the device geometries and trade-offs with power and circuit density go with the selection of these parameters.

SPICE Models

The devices available are the Schottky barrier diode, MESFET, HEMT and various passive components. While the existing diode and passive component SPICE models are adequate, the FET models require enhancement for application to GaAs FET's. In the current version of SPICE, the JFET and MESFET models were modified to obtain accurate predictions for MESFET's and HEMT's [5-6]. Second-order effects and careful matching of the small signal models have produced reliable models that can be used as a substitute for a fabrication test run.

Table I: Fundamental Fabrication Process Parameters			
Symbol	Default	Units	Description
Material dependent			
m^*/m	0.068	-	Relative electron mass in GaAs
N_c	+	cm^{-3}	Density of conduction states
ϵ_r	13.1	-	Relative permittivity
μ	+	$\text{cm}^2/\text{V/s}$	Low field drift mobility
E_m	+	V/cm	Maximum electron velocity field
v_m	+	cm/s	Maximum electron velocity
v_s	+	cm/s	Saturated electron velocity
Process dependent			
m_m/m	1.2	-	Rel. electron mass in Schottky metal
ϕ_m	3.38	eV	Work function of Schottky metal
ϕ_B	+	V	Schottky barrier height
r_s	150	Ω/sq	Epi layer sheet resistance
r_a	15	Ω/sq	Ohmic alloy sheet resistance
r_c	3000	$\Omega \cdot \mu\text{m}^2$	Metal to alloy contact resistance
L_t	+	μm	Ohmic contact transfer length
d_g	0.5	μm	Gate-drain and gate-source spacing
d_s	1.5	μm	Diode electrode spacing
Design dependent			
N_d	2×10^{17}	cm^{-3}	Nominal Doping Level
L	1	μm	MESFET gate length
a	+	\AA	MESFET channel depth
d_d	2.5	μm	Diode Schottky metal length
d_o	5	μm	Ohmic contact physical length
T	310	$^\circ\text{K}$	Temperature
+ denotes quantity calculated by <i>GaAsSPICE</i>			

The need for detailed modeling was critical because it was necessary to predict circuit behaviour using processes which had not yet been fully developed.

Gate Design Procedure

To automate the basic gate design procedure, a design sequence was developed which considers designer specified power/speed trade-offs and constraints on specification of power supplies, logic swings and circuit size. The sequence produces a parameterised topological description of a family of logic gates which can be passed to a parsing routine to create gate library subcircuits. These, in turn, are used in combination with designer trade-off goals to automatically design and layout each gate in the library. The SPICE models are reliably used as the basis for extracting device parameters used in the design sequence. An automatic SPICE-based procedure also uses the SPICE device models and gate subcircuit descriptions to derive a set of simple models for the Simulation JIG [7].

DESIGN SYSTEM IMPLEMENTATION

The design system is the bridge between the fabrication process and the set of model descriptions, standard circuit elements and layout cells. The core of the system is a PC-based front-end software package, *GaAsSPICE*, which maintains a database and provides an interface for designer interaction. Additional packages produce the Simulation Jig models and mask subcells (See Fig. 1).

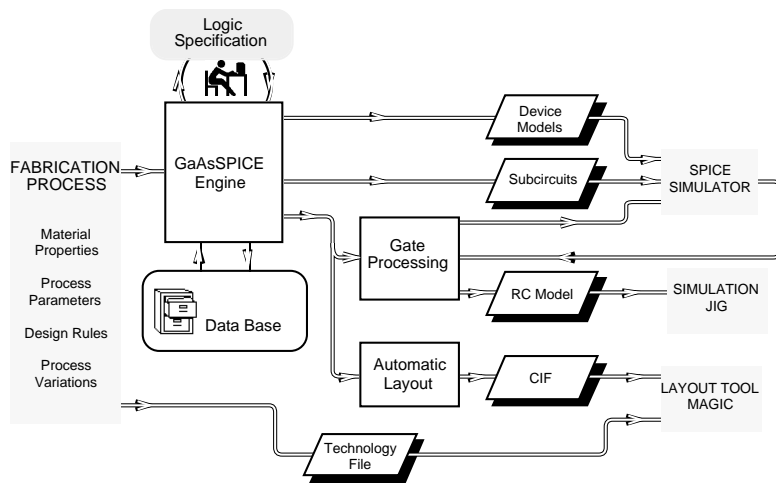


Figure 1. The Design System.

GaAsSPICE

GaAsSPICE has a highly modular structure in which a main engine invokes separate script files and calculation routines as needed. This flexible arrangement isolates independent design activities and facilitates rapid change of the design steps. For example, changes in circuit topology or subcircuit requirements are made simply by updating the appropriate script file. New simulators are accommodated by changing the parsing script to produce models in an appropriate format.

The fundamental process parameters are entered in three stages: the first for material properties, the second for process parameters (which are constant for a given process), and the third for design parameters.

From these are automatically generated accurate SPICE analogue device model descriptions suitable for use in the design of both linear and digital circuits. The user can enter the device characteristics or allow *GaAsSPICE* to calculate them from the fundamental parameters. Specifically, the diode and MESFET model parameters are listed with an option to over-ride each.

The device descriptions are used as an input to an automatic gate design system. At present this produces and stores in the database those parameters which give the ratio of device sizes within a BFL gate. The design parameters can be adjusted in

Logic Limits		max	nom	min
Logic High		+0.83	+0.35	-0.09
Logic Threshold		-0.24	-0.44	-0.82
Logic Low		-1.20	-1.37	-1.66

Figure 2. The logic gate design dialogue presented by *GaAsSPICE*

order to obtain the desired circuit performance.

The final step creates the SPICE 'include' files of gate libraries and model cards for various process settings and, additionally, produces a set of parameters which can be used by further processing routines to generate the JIG system level models and layout cells.

Calculation. *GaAsSPICE* performs a triple set of calculations to give models for a nominal condition, a high temperature extreme and a low temperature extreme. The designer can over-ride the nominal result and extreme cases are automatically calculated as a deviation from this result. The extreme case models are calculated from the set of extremes of parameter values specified in Table II.

Gate Design. An interactive gate design routine is used to produce a reference logic gate. The extreme of logic levels expected with process and environment variation are graphically given so that the user can check that the design parameters result in an effective circuit over all process and environment tolerances (See Fig. 2).

The design procedure uses simple piecewise approximations to the devices to iteratively design an optimum circuit based on dc logic levels and noise margins. The circuit is also optimised for maximum speed based on the user nominated fanout.

Symbol	Parameter	Low Model	High Model
T	Temperature	Low	High
r_a	Ohmic Alloy Sheet Resistance	Low	High
r_c	Ohmic Contact Resistance	Low	High
a	MESFET channel depth [†]	Low	High
N_d	Nominal doping Level	High	Low
d_s	Diode electrode spacing	Low	High
d_g	MESFET electrode spacing:		
	gate-drain	Low	High
	gate-source	High	Low

[†] The channel depth extremes are calculated from the pinch-off voltage variation and then the pinch-off variation used is calculated from the extremes of channel depth and doping.

RC Models

A system-level model is produced with the aid of a script program that drives SPICE and interprets its output. This uses a basic gate circuit to characterise each active component in the circuit. The transconductance and resistance of each device is approximated over its actual operating range and the device is substituted by a simple current source and conductance. The substituted devices in a basic gate are then assembled and simplified into a single current source and conductance for the gate. A parsing script is used to produce a listing of the simple models in an appropriate form for the Simulation JIG.

Mask Layout.

An automatic layout package uses the basic gate description produced by *GaAsSPICE* to create CIF subcells for each circuit in the model library. The cells follow a standard layout and the relative size of each component is adjusted as required. These subcells can be assembled with *Magic* and a set of process design rules is used for layout checking and circuit extraction.

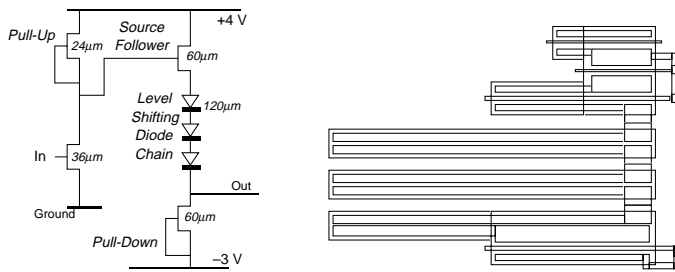


Figure 3. A inverter logic gate designed by *GaAsSPICE* and corresponding mask layout

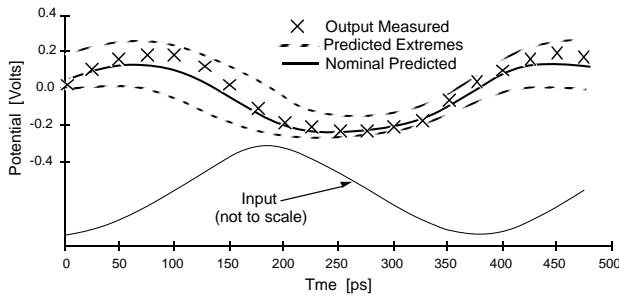


Figure 4. Measured and simulated ac response of the inverter shown in Fig. 3. Input is at 2.5 GHz and a 50 Ω output load was used.

EXAMPLE

The entire task from designer entry of parameters, through generation of accurate and simplified models, to layout, can be completed in less than 90 minutes. The inverter circuit shown in Fig. 3 was designed with *GaAsSPICE* using the parameters for a MBE mesa process developed at the CSIRO Division of Radiophysics [8]. The circuit models for the nominal and two extremes were used to simulate the responses shown in Figs. 4 & 5. A typical CIF layout is shown in Fig.3. The inverter was fabricated and the measured results are shown.

CONCLUSION

The design system presented here is a bridge between the fabrication process and a set of model descriptions, standard circuit elements and layout cells. It can be quickly adapted to a fundamental change in technology and therefore is a valuable *what if?* tool for determining the merits of a process modification. The designer may take up the design sequence at any stage and may freely over-ride internally calculated parameters.

User specified power/speed trade-offs and design constraints are used to automatically design and layout basic logic gates. SPICE models suitable for use in the design of both linear and digital circuits are generated and simplified models of the gates are extracted for use with the JIG mixed-mode simulator.

The design sequence is automated and can be easily repeated under the control of the PC-based front-end software package, *GaAsSPICE*. The modular structure of this package facilitates rapid change of the design steps. Thus, it will be a useful aid in the rapid application of new technologies.

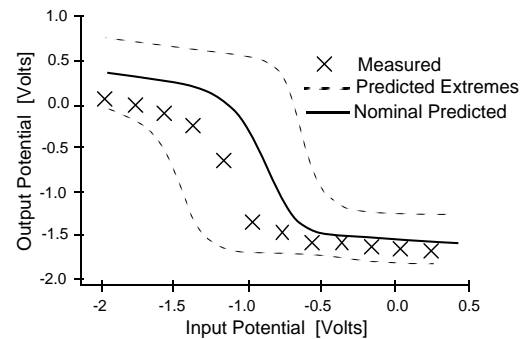


Figure 5. The dc transfer of the inverter in Fig. 3. Simulations were performed with SPICE using model cards created by *GaAsSPICE*

ACKNOWLEDGEMENT

This work is funded by a Commonwealth Scientific and Industrial Research Organisation (CSIRO) Collaborative Grant, The University of Sydney Research Grant, and The Australian Telecommunications and Electronics Research Board (ATERB). A.E.P. acknowledges the support of an Australian Commonwealth Postgraduate Research Award, a CSIRO Information Technology Scholarship, and an ATERB Postgraduate Scholarship.

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